UNITED STATES PATENT AND TRADEMARK OFFICE

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/037,129	01/04/2002	Arthur C. McKinney	1247/A63	5659

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EXAMINER
TRAN, DENISE

ART UNIT	PAPER NUMBER
2186	

DATE MAILED: 01/07/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE <u>3</u> MONTH(S) FROM
THE MAILING DATE OF THIS COMMUNICATION.
- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed
  after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any
  earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on <u>01 December 2003</u>.

2a)☐ This action is **FINAL**.   2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is
    closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) <u>4-10</u> is/are pending in the application.

　　4a) Of the above claim(s) <u>1-3 and 11-16</u> is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) <u>4-10</u> is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on <u>04 January 2002</u> is/are: a)☐ accepted or b)☒ objected to by the Examiner.

　　Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

　　Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. §§ 119 and 120

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

　　a)☐ All b)☐ Some * c)☐ None of:

　　　　1.☐ Certified copies of the priority documents have been received.

　　　　2.☐ Certified copies of the priority documents have been received in Application No. _____.

　　　　3.☐ Copies of the certified copies of the priority documents have been received in this National Stage
　　　　　　application from the International Bureau (PCT Rule 17.2(a)).

　　* See the attached detailed Office action for a list of the certified copies not received.

13)☒ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application)
    since a specific reference was included in the first sentence of the specification or in an Application Data Sheet.
    37 CFR 1.78.

　　a)☐ The translation of the foreign language provisional application has been received.

14)☒ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121 since a specific
    reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

Attachment(s)

1)☒ Notice of References Cited (PTO-892)　　　　　　　　　4)☐ Interview Summary (PTO-413) Paper No(s). _____.

2)☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)　5)☐ Notice of Informal Patent Application (PTO-152)

3)☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) <u>3</u>.　6)☐ Other: .

DETAILED ACTION

1.   Claims 1-3 and 11-16 are withdrawn from further consideration pursuant to 37 CFR 1.142(b) as being drawn to a nonelected invention, there being no allowable generic or linking claim. Election was made **without** traverse in Paper No. 6.

2.   Applicant's election without traverse of claims 4-10 in Paper No. 6 is acknowledged.

3.   Claims 4-10 are presented for examination.

4.   The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

5.   The disclosure is objected to because of the following informalities: the status of the parent application on page 1 of the specification should be updated.

Appropriate correction is required.

6.   The amendment filed 1/4/92 or 12/1/03 is objected to under 35 U.S.C. 132 because it introduces new matter into the disclosure. 35 U.S.C. 132 states that no amendment shall introduce new matter into the disclosure of the invention. The added material which is not supported by the original disclosure is as follows: "each processor has an internal cache which is externally unreadable outside the processor," claim 7,

lines 4-5; performing a snoop cycle on the processor bus of the second segment if the

second segment has a reference to the requested data," claim 7, lines 10-11; and

"sending the requested data to the requesting processor from a processor in the second

segment if the snoop cycle returns a signal indicating the processor of the second

segment has modified the requested data, claim 9, lines 2-4 "recalling from main

memory . . . if all of the application specific integrated circuits . . . fail to have a

reference to the requested data" claim 10, line 1-3; and claim 4 contains the similar

problems as discussed above.

Applicant is required to cancel the new matter in the reply to this Office Action.

7.   The drawings are objected to under 37 CFR 1.83(a). The drawings must show

every feature of the invention specified in the claims. Therefore, the "each processor

has an internal cache which is externally unreadable outside the processor," claim 7,

lines 4-5; performing a snoop cycle on the processor bus of the second segment if the

second segment has a reference to the requested data," claim 7, lines 10-11; and

"sending the requested data to the requesting processor from a processor in the second

segment if the snoop cycle returns a signal indicating the processor of the second

segment has modified the requested data, claim 9, lines 2-4 "recalling from main

memory . . . if all of the application specific integrated circuits . . . fail to have a

reference to the requested data" claim 10, line 1-3; performing a snoop cycle on the

second processor if the external cache has a reference to the requested data ; and

determining if the requested data has been modified in the second processor" claim 4;

"sending to the requesting processor from the second processor the requested data if

the second processor has modified the requested data" claim 5 must be shown or the

feature(s) canceled from the claim(s). No new matter should be entered.

A proposed drawing correction or corrected drawings are required in reply to the Office

action to avoid abandonment of the application. The objection to the drawings will not

be held in abeyance.

8.   Claims 5-6 and 8-10 are objected to because of the following informalities: "a

method" claim 5, line 1 should be –The method--; "the requesting processor" claim 5,

line 3 should be --a requesting processor--; "theexternal" claim 6, line 4 should be –the

external--; "a method" claim 6, line 1 should be –The method--; "the segment" should be

–the segments--; "a method" claim 10, line 1 should be –The method--; "the application

specific integrated circuits" claim 10, line 3 should be -- application specific integrated

circuits--; and claims 8-9 contain similar problems as discussed in claims 5, 6, and 10

above. Appropriate correction is required.

9.   The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of
> making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the
> art to which it pertains, or with which it is most nearly connected, to make and use the same and shall
> set forth the best mode contemplated by the inventor of carrying out his invention.

10.   Claims 4-10 are rejected under 35 U.S.C. 112, first paragraph, as failing to

comply with the written description requirement. The claim(s) contains subject matter,

which was not described in the specification in such a way as to reasonably convey to

one skilled in the relevant art that the inventor(s), at the time the application was filed,

had possession of the claimed invention. In particular, "each processor has an internal

cache which is externally unreadable outside the processor," claim 7, lines 4-5;

performing a snoop cycle on the processor bus of the second segment if the second

segment has a reference to the requested data," claim 7, lines 10-11; and "sending the

requested data to the requesting processor from a processor in the second segment if

the snoop cycle returns a signal indicating the processor of the second segment has

modified the requested data, claim 9, lines 2-4 "recalling from main memory . . . if all of

the application specific integrated circuits . . . fail to have a reference to the requested

data" claim 10, line 1-3; and claim 4 contains the similar problems as discussed above;

Which were not described in the specification in such a way as to reasonably convey to

one skilled in the relevant art that the inventor(s), at the time the application was filed,

had possession of the claimed invention.

11.   The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly
> claiming the subject matter which the applicant regards as his invention.

12.   Claims 4-10 are rejected under 35 U.S.C. 112, second paragraph, as being

indefinite for failing to particularly point out and distinctly claim the subject matter which

applicant regards as the invention.

As per claim 4, line 1, it is unclear whether "main memory" directs to the main

memory of claim 1, line 2 or an addition main memory because according to fig. 1, there

are more than one memory, e.g., memories 112, 114;

As per claim 7, it is unclear whether "main memory" directs to the main memory

of claim 1, line 2 or an addition main memory because according to fig. 1, there is more

than one memory, e.g., 112, 114; it is unclear whether "the processor bus of the second

segment" directs to "the processors connected together by a processor bus" of claim 7,

lines 2-3 or direct to an addition processor bus because as seen from fig. 2, each

segment has its own processor bus.

13.   The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all

obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set
> forth in section 102 of this title, if the differences between the subject matter sought to be patented and
> the prior art are such that the subject matter as a whole would have been obvious at the time the
> invention was made to a person having ordinary skill in the art to which said subject matter pertains.
> Patentability shall not be negatived by the manner in which the invention was made.

14.   Claims 4-10 are rejected under 35 U.S.C. 103(a) as being unpatentable over

Morioka et al., U. S. Patent No. 6,631,447, (hereinafter Morioka) in view of Official

Notice.

As per claims 7 and 4, Morioka shows a method for maintaining coherent data in

a multiprocessor system having a plurality of processors forming a segment, the

processors connected together by a processor bus and the segment connected

together by a system bus which is coupled to main memory, where each processor has

an internal cache which is externally unreadable outside the processor (e.g., abstract

and figs. 1-2), the method comprising:

placing a request from a processor in a first segment for data associated with a

memory location in main memory on the system bus (e.g., fig. 8, el. 909; col. 13, lines

25-30);

determining if an external cache coupled to any circuit associated with a second

segment contains a reference to the requested data (e.g., fig. 8, el. 911; col. 13, lines

35-55)

performing a snoop cycle on the processor bus of the second segment if the

second segment has a reference to the requested data (e.g., col. 11, lines 44-55; col.

12, lines 14-24; col. 25, lines 55-65);

determining if the requested data has been modified in the second processor

(e.g., col. 11, lines 50-55; col. 15, lines 42-45; col. 25, lines 65-67). Morioka does not

explicitly shows the use of application specific integrated. "Official Notice" is taken that

both the concept and the advantages of providing application specific integrated are

well known and expected in the art. It would have been obvious to one of ordinary skill

in the art at the time the invention was made to provide application specific integrated

circuits to the system of Morioka because it would allow manufacturer to make a circuit

suitable for many needs, thereby saving both design and manufacturing time.

As per claims 8-9 and 5-6, Morioka shows determining if the requested data has

been modified (e.g., col. 11, lines 50-55; col. 15, lines 42-45; col. 25, lines 65-67);

sending the requested data to the requesting processor from a processor in the second segment if the snoop cycle return a signal indicating the processor of the second segment has modified the requested data (e.g., col. 11, lines 44-55; col. 12, lines 14-24; col. 25, lines 55-65); and recalling from main memory the data associated with a memory location in main memory if the external cache fails to have a reference to the requested data (e.g., col. 15, lines 30-55; col. 15, line 60 to col. 16, line 2; and col. 17, lines 20-42).

As per claim 10, Morioka shows recalling from main memory the data associated with a memory location in main memory if all of the circuits associated with a segment fail to have a reference to the requested data (e.g., col. 15, lines 30-55; col. 15, line 60 to col. 16, line 2; and col. 17, lines 20-42). Morioka does not explicitly shows the use of application specific integrated. "Official Notice" is taken that both the concept and the advantages of providing application specific integrated are well known and expected in the art. It would have been obvious to one of ordinary skill in the art at the time the invention was made to provide application specific integrated circuits to the system of Morioka because it would allow manufacturer to make a circuit suitable for many needs, thereby saving both design and manufacturing time.

15.   The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

a)   Blake et al. (5752264) shows processor clusters having cache memories and snooping;

b)   Sell (5860114 shows reducing snoops of a processor's internal cache.

16.   Any inquiry concerning this communication or earlier communications from the examiner should be directed to Denise Tran whose telephone number is (703) 305-9823. The examiner can normally be reached on Monday, Thursday and an alternated Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matt Kim can be reached on (703) 305-3821. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 872-9306 for central Official communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 305-3900.

Denisepan

D.T.
January 5, 2004